TIME TABLE - II SEMESTER

VLSI DESIGN

	9.30-10.30	11.00-12.00	12.00-1.00	1.00-2.00	2.00-3.00	3.00-4.00	4.00-5.00
Monday	ASIC(AN)-41	TFT(MK)-41	ES(BS)-41		ADSP(VS)-41	FPGA LAB(MK)- 40/40A	
Tuesday	TFT(MK)-41	ASIC(AN)-41	ES(BS)-41		MDT(BS/AN)-41	ES LAB(BS)-40/40A	
Wednesday	MDT(BS/AN)-41	ADSP(VS)-41	TFT(MK)-41		ES(BS)-41	FPGA LAB(MK)- 40/40A	
Thursday	ADSP(VS)-41	MDT(BS/AN)-41	ASIC(AN)-41		TFT(MK)-41	ES LAB(BS)-40/40A	
Friday	ES(BS)-41	MDT(BS/AN)-41	ADSP(VS)-41		ASIC(AN)-41		

EMBEDDED SYSTEMS (ES)

	9.30-10.30	11.00-12.00	12.00-1.00	1.00-2.00	2.00-3.00	3.00-4.00	4.00-5.00
Monday	RTS(PB)-41A	AMPMC(HP)-41A	ES(BS)-41		CA(VC/MU)-41A	RTOS LAB(PB)-41A	
Tuesday	NNFL(SS)-41A	CA(VC/MU)-41A	ES(BS)-41		RTS(PB)-41A	AMPMC LAB(MU) -41A	
Wednesday	AMPMC(HP)-41A	NNFL(SS)-41A	CA(VC/MU)-41A		ES(BS)-41	RTOS LAB(PB)-41A	
Thursday	CA(VC/MU)-41A	RTS(PB)-41A	NNFL(SS)-41A		AMPMC(HP)-41A	AMPMC LAB(MU) -41A	
Friday	ES(BS)-41	RTS(PB)-41A	AMPMC(HP)-41A		NNFL(SS)-41A		

BS :	Dr. Balwinder Singh
MK :	Ms. Manjit Kaur
VS :	Ms. Vemu Sulochana
PB :	Mr. Prashant Bhardwaj
AN :	Mr. Anurag
VC :	Mr. Varun Chhabra
SS :	Mr. Satbir Singh
HP :	Mr. Hitesh Pahuja